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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/823,060	04/13/2004	Wei Fu	AMCC10180	3987

7590 10/20/2005

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EXAMINER	
NGUYEN, MINH T	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 10/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/823,060	FU ET AL.	
	Examiner	Art Unit	
	Minh Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 September 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 3-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,6,7,11 and 16* is/are rejected.

7)☒ Claim(s) *3-5,8-10,12-15 and 17-20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Applicant's amendment filed on 9/26/05 has been received and entered in the case. The amendment and argument presented therein overcome the informality objections and prior art rejections, therefore, these are withdrawn. However, new grounds of rejections (new interpretations based on the same prior art used in the previous Office action) necessitated by the amendment are needed as set forth below. This action is FINAL.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 6-7, 11 and 16 are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent No. 5,799,048, issued to Farjad-Rad et al.

As per claim 6, Farjad discloses a half-rate phase detector (figure 3) for indicating a phase difference between an incoming data signal (DATA) and a clock signal (CLK1) synthesized from the incoming data signal (using a PLL structure to synthesize), comprising:

a first latch circuit (latch 40) for combining a first delayed version of the incoming data signal (D1 is the first delayed version of the DATA signal) with alternate transitions of a first

delayed version of the clock signal (signal CLK2 is the first delayed version of the clock signal CLK1 by delay element 44) to produce first precursor signals (DA2);

a multiplexer (MUX 46) connected to the first latch circuit (first latch 40 is connected to MUX 46) for multiplexing the first precursor signals (MUX 46 receives the first precursor signals DA2) in response to a second delayed version of the clock signal (the clock signal CLK1 is delayed by delay elements 44 and 48) to produce a multiplexed signal (the signal D2), the multiplexer including an output for providing the multiplexed signal to a single input (the output of MUX 46 provides the D2 signal to only the first input of the XOR gate 18);

a first logic gate (XOR gate 18) with a first input (the input which receives the signal D2) connected to the multiplexer output (the multiplexer 46 outputs D2 to the first input of the XOR gate 18) and a second input for receiving a second delayed version of the incoming data signal (the incoming data signal DATA is delayed by delay element 52 before the DATA signal is fed to the second input of the XOR gate 18) for combining the multiplexed signal (D2) with a second delayed version of the incoming data signal (D1') to produce a phase signal (X2) indicative of a phase difference between the incoming data signal and the clock signal.

As per claim 7, the recited first XOR gate reads on the XOR gate 18.

As per claim 11, Farjad discloses half-rate phase detector (figure 3) for detecting a phase difference between a data signal and a clock signal, comprising:

an input for receiving the data signal (node which receives the signal DATA);

a first latch (latch 40) for sampling a first delayed version of the data signal (D1 is the first delayed version of the data signal DATA) in response to a first delayed version of the clock

signal (CLK2 is the first delayed version of the clock signal CLK1, delay element 44), the first latch having an output (output Q of latch 40, the signal DA2);

a second latch (latch 42) for sampling the first delayed version of the data signal (the data signal D1) in response to the inverse of the first delayed version of the clock signal (/CLK2), the second latch having an output (output Q of latch 42, the signal DB2);

a multiplexer (MUX 46) having a first input connected to the output of the first latch (DA2), a second input connected to the output of the second latch (DB2), a control input for receiving a second delayed version of the clock signal (clock CLK1 is delayed by delay elements 44 and 48), and an output (D2); and

a first exclusive-OR gate (XOR 18) having a first input connected to the output of the multiplexer (D2), a second input for receiving a second delayed version of the data signal (the delay circuit 52 generates the second delayed version of the date signal), and an output for producing a phase signal (X2) representing a phase difference between the data signal and the clock signal;

the multiplexer output being connected only to the first input of the XOR gate (only the first input of XOR gate 18 receives the D2 signal).

As per claim 1, this claim is merely a method to operate the phase detector having the structure discussed in claim 6. Since Farjad teaches the structure, the method to operate is inherently taught.

As per claim 16, this claim is merely a method to operate the phase detector having the structure discussed in claim 11. Since Farjad teaches the structure, the method to operate is inherently taught.

Response to Arguments

3. Applicant's arguments with respect to the claims have been considered but are moot in view of the new ground(s) of rejection.

Allowable Subject Matter

4. Claims 3-5, 8-10, 12-15 and 17-20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 8-10 are allowable because the prior art of record fails to disclose or suggest the inclusion of a second logic gate for combining the second precursor signals to produce a reference signal as recited in claim 8. The recited limitation defines patentability over the prior art of record because it defines a distinguished structure of the phase detector which is not taught by the art of record, alone or in combination.

Claims 3-5, 12-15 and 17-20 are allowable for the same reason noted in claim 8.

Conclusion

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO

MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Minh Nguyen whose telephone number is **571-272-1748**. The examiner can normally be reached on Monday, Tuesday, Thursday, Friday 7:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

10/17/05

Minh Nguyen
Primary Examiner
Art Unit 2816